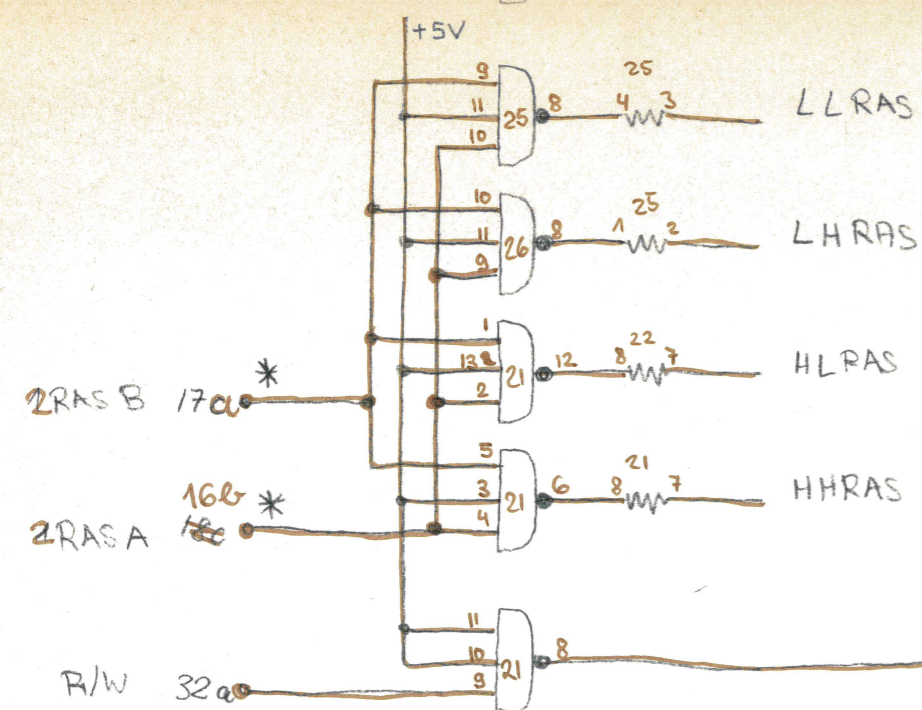
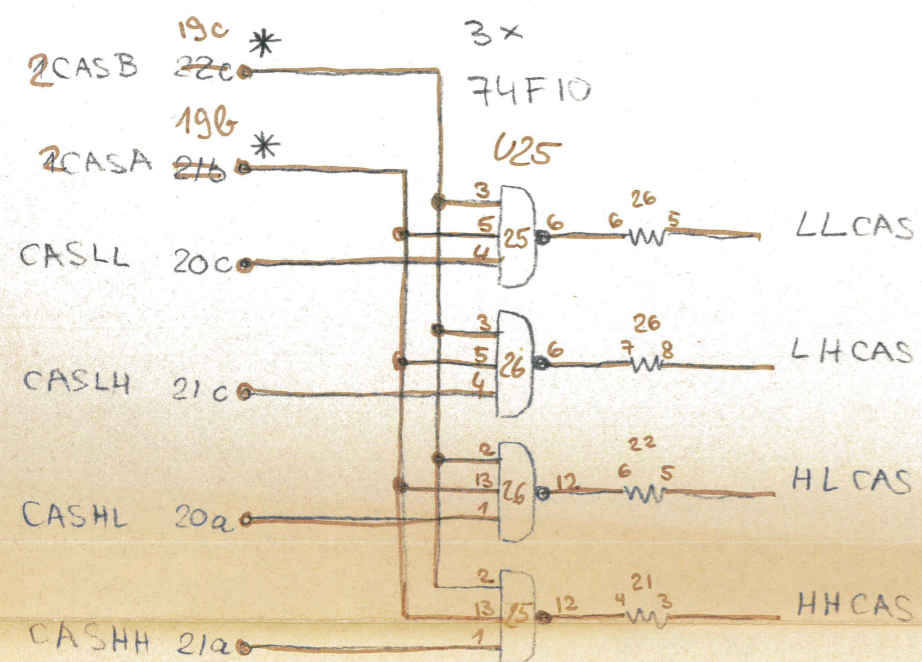
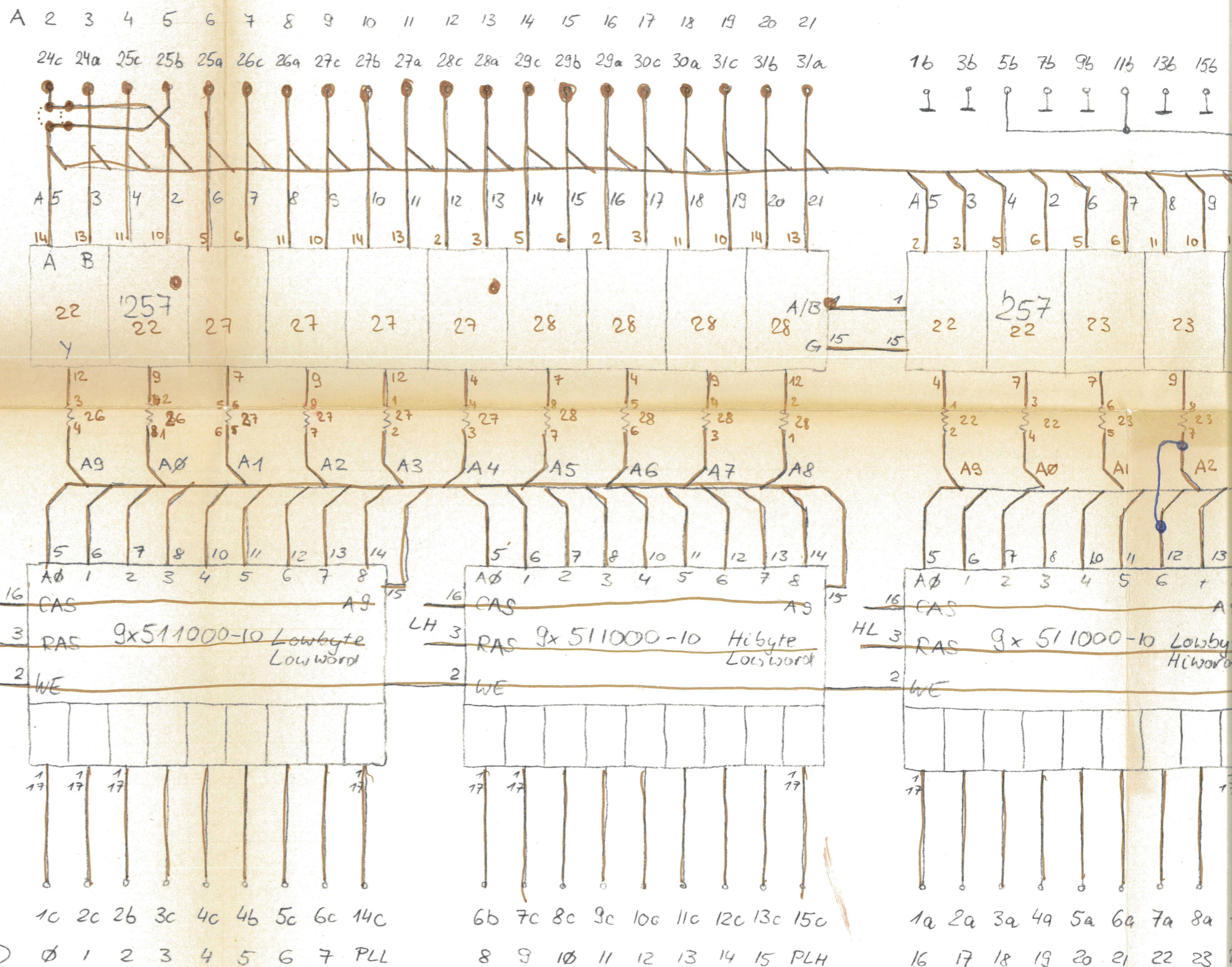


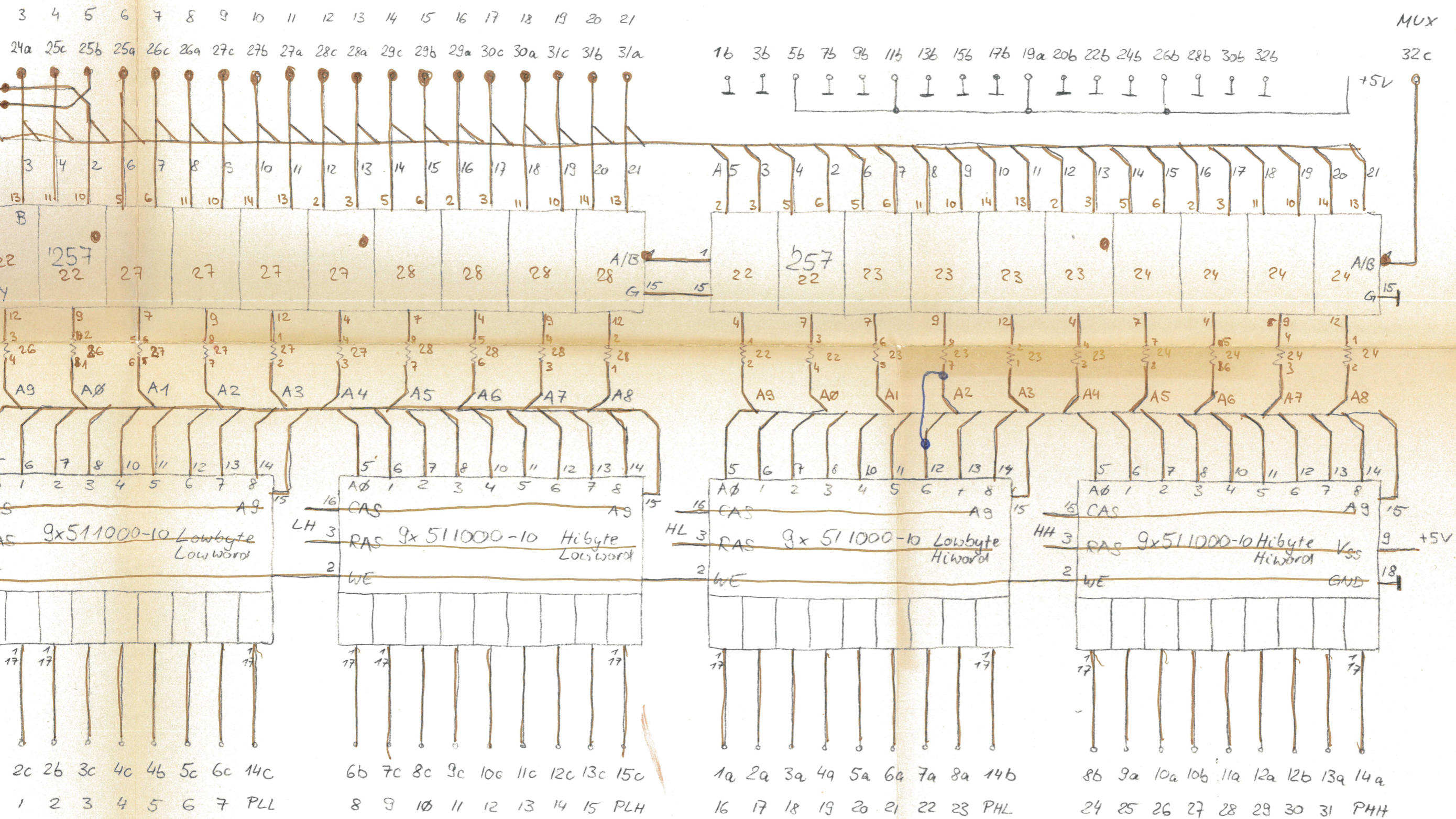
②



- 2CASB 19c *
- 2CASA 19b *
- 2RASB 17a *
- 2RASA 16b *
2. 4MB-Block
- 3CASB 22a *
- 3CASA 22b *

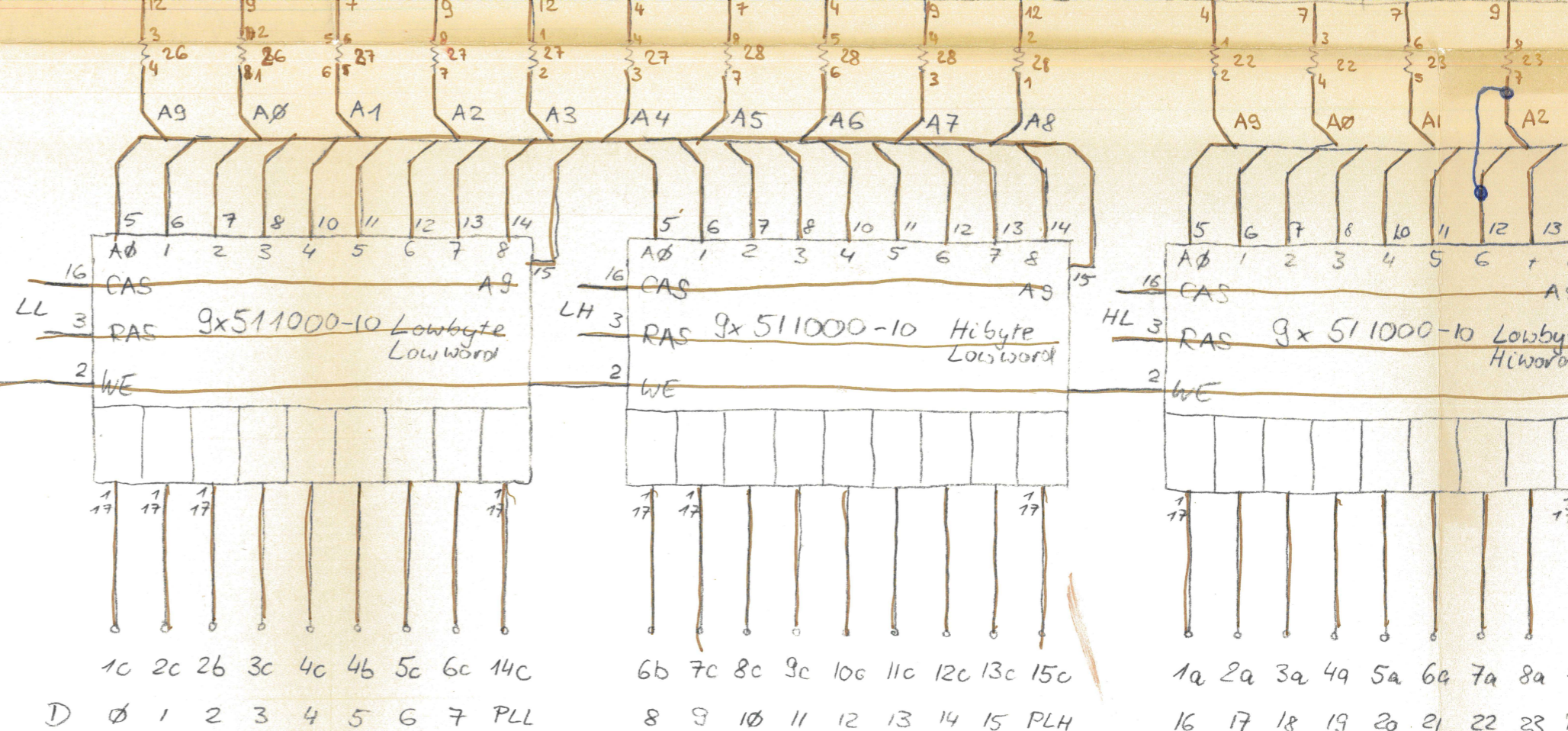
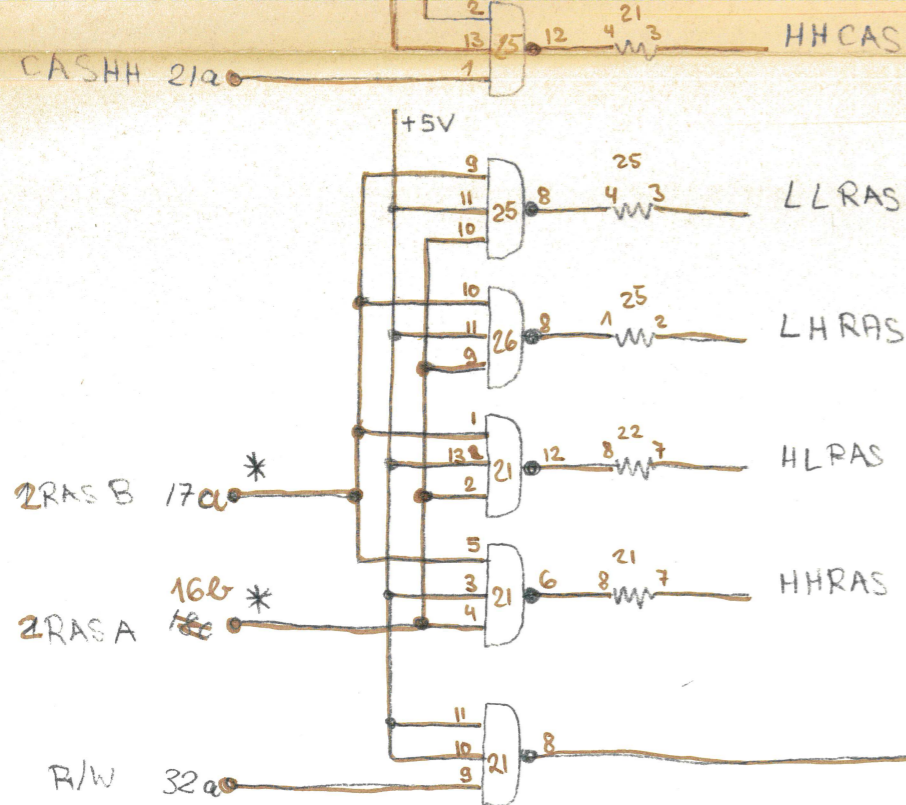


Pin	A	B	C
1	D16	GND	D0
2	D17	D2	D1
3	D18	GND	D3
4	D19	D5	D4
5	D20	+5V	D6
6	D21	D8	D7
7	D22	GND	D9



Pin	A	B	C
1	D16	GND	D0
2	D17	D2	D1
3	D18	GND	D3
4	D19	D5	D4
5	D20	+5V	D6
6	D21	D8	D7
7	D22	GND	D9

②



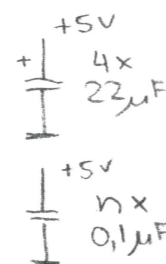
~~2CASH 19c *~~
~~2CASA 19b *~~
~~2RASB 17a *~~
~~2RASA 16b *~~

2. 4MB-Block

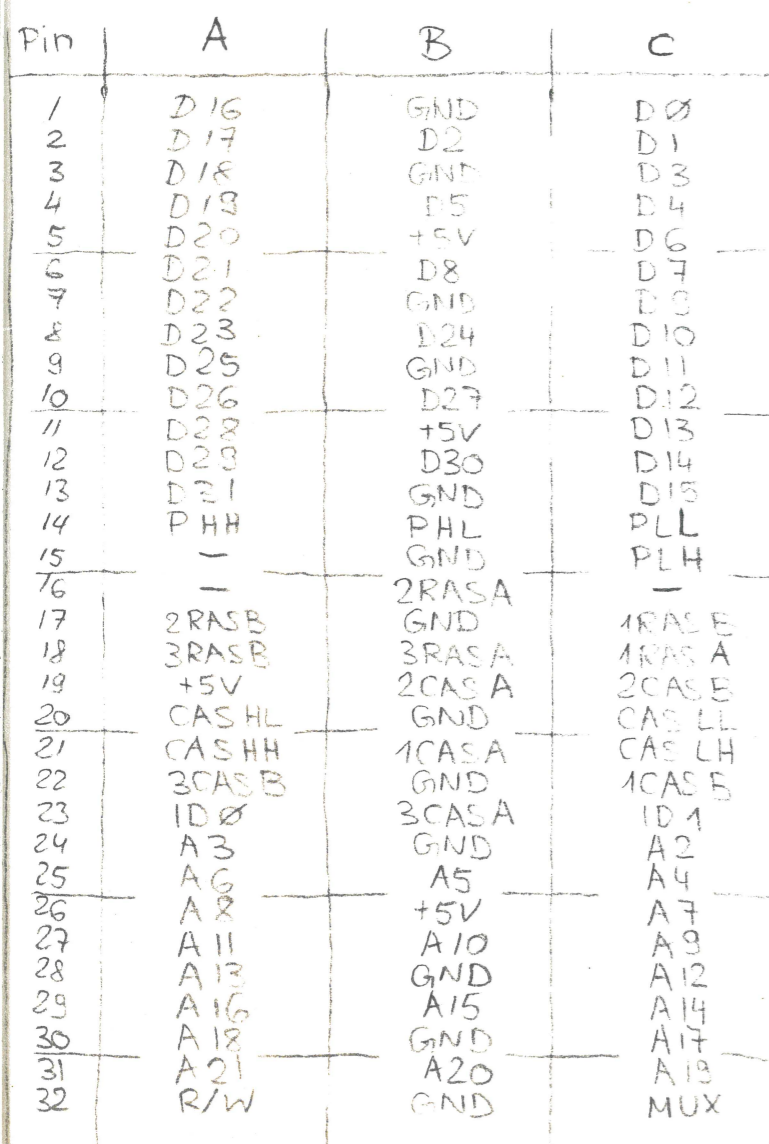
~~3CASH 22a *~~
~~3CASA 23b *~~
~~3RASB 18a *~~
~~3RASA 18b *~~

3. 4MB-Block

~~ID0 23a *~~ JMP=4MB
~~ID1 23c *~~ JMP=12MB

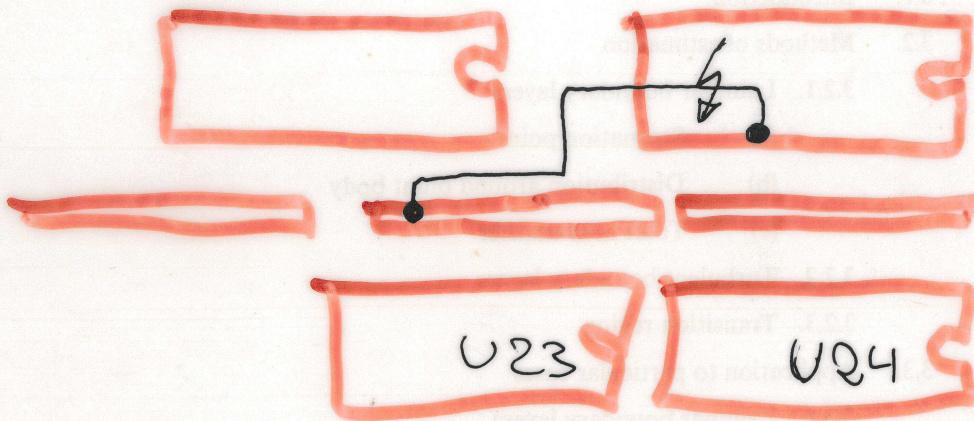
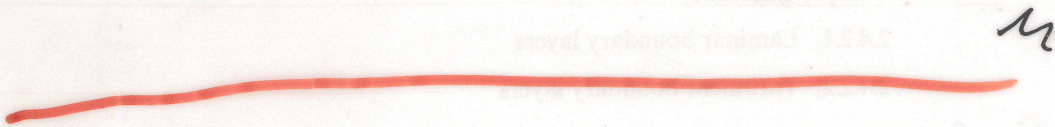
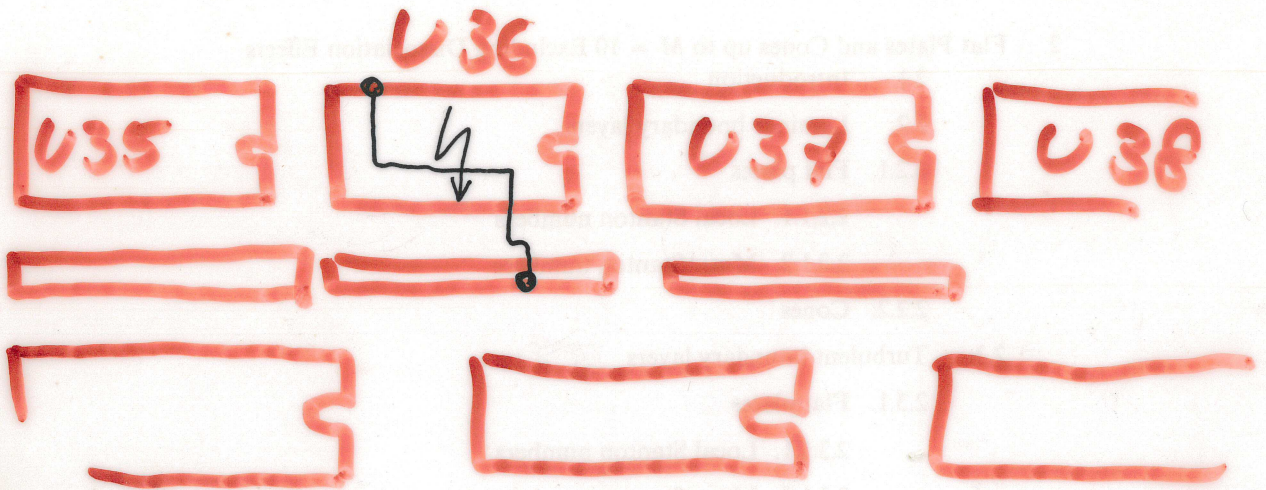


Pin	A	B	C
1	D16	GND	D0
2	D17	D2	D1
3	D18	GND	D3
4	D19	D5	D4
5	D20	+5V	D6
6	D21	D8	D7
7	D22	GND	D9
8	D23	D24	D10
9	D25	GND	D11
10	D26	D27	D12
11	D28	+5V	D13
12	D29	D30	D14
13	D31	GND	D15
14	PHH	PHL	PLL
15	-	GND	PLH
16	-	-	-
17	2RASB	GND	1RASB
18	3RASB	3RASA	1RASA
19	+5V	2CASA	2CASB
20	CASHL	GND	CASLL
21	CASHH	1CASA	CASLH
22	3CASB	GND	1CASB
23	ID0	3CASA	ID1
24	A3	GND	A2
25	A6	A5	A4
26	A8	+5V	A7
27	A11	A10	A9
28	A13	GND	A12
29	A16	A15	A14
30	A18	GND	A17
31	A21	A20	A19
32	R/W	GND	MUX



Für diese Zeichnung gelten die Bestimmungen über den Schutz für Urheberrecht

MEM 4/12 COMPO 1



bei 12 MByte hier \downarrow
 unterbrechen unter'm IC!
 (Absichtliche Kurzschlüsse gegen Erweiterung
 4 \rightarrow 12 durch Nachbestücken)